REMARKS

In the Office Action the Examiner noted that claims 1-14 are pending in the application and the Examiner rejected all claims. By this Amendment, claims 1 and 11-13 have been amended, claims 9-10 and 14 have been cancelled, and new claims 15-16 have been added. Thus, claims 1-8, 11-13, and 15-16 are pending in the application. The Examiner's rejections are traversed below.

Rejections under 35 U.S.C. §102

In items 3-9 on pages 2-5 of the Office Action the Examiner rejected claims 1-6 and 14 under 35 U.S.C. §102(b) as being anticipated by Faraboschi et al., U.S. Patent Number 5,930,508 (hereinafter referred to as "Faraboschi"). By this Amendment, claim 14 has been cancelled.

In regard to claim 1, the Examiner cites Faraboshci as teaching "a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising (Faraboschi figures 4 and 5 abstract column 3 lines 16-25): [a] plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48); [an] instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36, the alignment logic 720 acts as the fetch unit); and [an] instruction issue unit recognizing and, in accordance therewith, selectively [issuing] each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction (Faraboshci column 3 lines 25-32, column 4 line 57-column 5 line 11)."

Therefore, Faraboshci teaches attaching a set of dispersal bits to each basic instruction of a compacted instruction set and sending the basic instructions to corresponding functional units according to the dispersal bits (Column 4, line 57 through Column 5, line 11). Each compacted instruction word includes "words containing an operation code, a dispersal code, and a delimiter code" (Column 3, lines 15-25), and "dispersal means transfers each word of the compacted instruction stored in the alignment buffer into at least one operational field of the

executable instruction responsive to the dispersal code corresponding to the word" (Column 3, lines 25-32). Thus, the instruction words gathered and executed by the processor in Faraboshci contain dispersal codes along with the executable instruction and delimiter information.

Amended claim 1 of the present invention recites:

> A parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising:
> a plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel;
> an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information; and
> an instruction issue unit recognizing and, in accordance therewith, selectively issuing each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction;
> wherein the instruction issue unit comprises a conversion unit to generate an interface having effective bits and instruction information based on the instruction words, the effective bits indicating availability of the corresponding instruction execution units and the instruction information indicating a type of the corresponding instruction execution units.

Therefore, the parallel processor of the claimed invention includes "a conversion unit to generate an interface having effective bits and instruction information based on the instruction words, the effective bits indicating availability of the corresponding instruction execution units and the instruction information indicating a type of the corresponding instruction execution units." This is in direct contrast to Faraboschi, which apparently has no such "conversion unit to generate an interface having effective bits and instruction information based on the instruction words," but instead merely disperses instruction words according to dispersal codes that have already been attached to the instruction words themselves before being fetched by an instruction fetch unit. As a result, in Faraboschi, a given basic instruction has to be supplied to a functional unit indicated by the attached dispersal code, no matter where this basic instruction is located within the compacted instruction set. This requires excessive hardware such as a crossbar switch. In comparison, the conversion unit of the claimed invention supplies an interface which makes it possible to specify a selection of the instruction execution units to which the basic instructions are to be issued without having dispersal codes pre-attached to the instruction words, which reduces hardware size and requirements.

Accordingly, it is submitted that Faraboschi does not disclose every element of the Applicants' claim 1. In order for a document to anticipate a claim, the document must teach each and every element of the claim (MPEP §2131). Therefore, since Faraboschi does not teach the features recited in independent claim 1, as stated above, it is respectfully submitted

that claim 1 patentably distinguishes over Faraboschi, and withdrawal of the §102(b) rejection is earnestly and respectfully solicited.

Claims 2-6 depend from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by Faraboschi. Therefore, it is submitted that claims 2-6 also patentably distinguish over the prior art.

Rejections under 35 U.S.C. §103

In items 10-12 on pages 5-7 of the Office Action the Examiner rejected claims 7-8 under 35 U.S.C. §103(a) as being unpatentable over Faraboschi in view of Nair et al., "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups."

Claims 7-8 depend from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by the prior art. As discussed above, independent claim 1 contains features that are not found in Faraboschi, and the deficiencies of Faraboschi are not cured by Nair. Therefore, it is respectfully submitted that claims 7-8 also patentably distinguish over the prior art.

In items 13-18 on pages 7-9 of the Office Action the Examiner rejected claims 9-13 under 35 U.S.C. §103(a) as being unpatentable over Faraboschi in view of Park et al., U.S. Patent Number 5,881,307.

Claims 9-13 depend from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by the prior art. As discussed above, independent claim 1 contains features that are not found in Faraboschi, and the deficiencies of Faraboschi are not cured by Park. Therefore, it is respectfully submitted that claims 9-13 also patentably distinguish over the prior art.

New claims 15-16

New claim 15 depends from claim 1 and includes all of the features of that claim plus additional features which are not taught or suggested by the prior art. Therefore, it is respectfully submitted that new claim 15 also patentably distinguishes over the prior art.

New independent claim 16 recites the features of "an interface having effective bits corresponding to the instruction execution units, the effective bits indicating the corresponding instruction execution unit for each instruction word; wherein the instruction words fetched by the

instruction fetch unit have no attached dispersal information." Neither Faraboschi, Nair, nor Park, taken alone or in combination, teaches or suggests these features. Therefore, it is respectfully submitted that claim 16 also patentably distinguishes over the prior art.

Summary

It is submitted that none of the references either taken alone or in combination teach the present claimed invention. Thus claims 1-8, 11-13, and 15-16 are respectfully deemed to be in condition for allowance. Reconsideration of the claims and an early notice of allowance are earnestly solicited.

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 01/15/04

By: Thomas L. Jones
Thomas L. Jones
Registration No. 53,908

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

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STAAS & HALSEY
By: D. Strain
Date: 1-15-04